Gate Oxide Degradation Condition Monitoring Technique for High-Frequency Applications of Silicon Carbide Power MOSFETs

Javad Naghibi, *Student Member, IEEE*, Sadegh Mohsenzade, *Member, IEEE*, Kamyar Mehran, *Senior Member, IEEE*, and Martin P. Foster

***Abstract*—Gate oxide degradation, which considerably affects turn-ON/-OFF dynamics of the switch, embraces a large percentage of chip-related failure modes both in silicon and silicon carbide power MOSFETs. The gate oxide layer is thinner in silicon carbide power MOSFETs in comparison to their silicon-based counterparts. Consequently, the problem of gate oxide degradation has become a more crucial impediment in achieving reliable performance in silicon carbide power MOSFETs. This problem is even more severe in high-frequency applications due to higher EMI signature and complicated and costly measurement. In this article, a reliable fully analog cost-effective gate oxide degradation condition monitoring technique is proposed and validated. High-order harmonics magnitudes of drain–source voltage are used to produce a dc signal as the aging precursor of the gate oxide region. Using a dedicated degradation setup, the credibility of the developed condition monitoring technique was examined at different rates of gate oxide degradation for 650-V/22-A silicon carbide discrete MOSFET. In 200-kHz, 217-V switch operation, the proposed precursor showed 68% change in comparison to its initial value. This brings a high-resolution assessment on the reliability level of the switch gate oxide region.**

***Index Terms*—Condition monitoring (CM), frequency spectrum, gate oxide degradation, reliability, wide bandgap.**

I. Introduction

WIDE-BANDGAP-based power switches, specifically silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs), can provide the required high-power, high-frequency, and high-temperature operation for the next generation power electronic applications [1], [2], [3], [4], [5], [6], [7], [8]. Achieving reliable performance, however, is a fundamental requirement, which still should be addressed further in SiC power MOSFET switches [2], [3], [9]. Package-level (wire bond-related and solder-related degradation modes) and chip-level (gate-oxide-related and body-diode-related degradation modes) have been distinguished as the two main classes of reliability issues in SiC MOSFETs [10]. Gate oxide degradation is typically caused by the tunneling current into the gate oxide layer [10]. A gate oxide layer, which is mainly from SiO_2 material, is considerably thinner in SiC MOSFETs compared to the silicon (Si) counterparts to provide acceptable threshold voltage ($V_{\rm th}$) and transconductance (g_{fs}) values [2], [11]. Poor quality of SiC/SiO_2 interface can further lead to low inversion layer mobility in SiC MOSFETs [5]. Moreover, the smaller conduction band offset between SiC and SiO_2 permits higher leakage current and smaller breakdown field value in SiC MOSFET gate oxide compared to Si MOSFETs [4]. Therefore, there are critical vulnerabilities against gate oxide degradation and breakdown in SiC power MOSFET devices.

Different condition monitoring (CM) techniques have been recently suggested [1], [8], [12], [13], [14], as passive reliability assessment methods for chip-level degradation in SiC MOSFETs. $V_{\rm th}$ [15], drain leakage current [16], gate leakage current [3], gate-plateau voltage ($V_{\rm GP}$) [17], Miller gate-plateau time ($t_{\rm GP}$) [11], switch turn-ON delay [6], switch junction capacitance [18], ON-state resistance ($R_{\rm DS-on}$) [19], etc., have been used as CM precursors in the literature. The employed failure precursors, which are generally adopted from the conventional Si-based MOSFETs [11], sometimes behave differently during the SiC MOSFET gate oxide degradation process in comparison to the ones of Si MOSFETs. For example, in [11], it is shown that there is a rebound in a $t_{\rm GP}$ value during degradation of Si-based MOSFETs while this parameter experiences a steady increasing trend during SiC MOSFET gate oxide degradation [11]. In other cases, $V_{\rm th}$ instability is reported during SiC MOSFET gate oxide degradation, which is basically due to electron injection into gate oxide traps during gate oxide degradation [1], [3], [5]. Therefore, specialized failure precursors are required for the assessment of gate oxide degradation in SiC MOSFETs [6]. Employing the existing SiC MOSFET gate oxide failure indicators for the switch operation in high-frequency and high-voltage operating conditions has the following problems.

1) Measurement of the switch operational parameters, i.e., $V_{\rm th}$, $R_{\rm DS-on}$, $V_{\rm GP}$, and $t_{\rm GP}$ for reliability assessment purposes

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requires complicated implementation techniques. Using $V_{\rm th}$ as a degradation indicator, for example, requires high sensing speed for both drain current and gate–source voltage ($V_{\rm GS}$) of the switch [6]. Besides, for using time-based degradation precursors such as $t_{\rm GP}$, an analog-to-digital converter (ADC) module is required to capture $V_{\rm GS}$ waveform during the switch's turn-ON transient, which basically faces limitations in ADC bandwidth and electromagnetic interference (EMI) problems [6]. Specifically, in high switching frequency converters (+20 kHz), due to a higher rate of di/dt, the EMI signature is increased considerably, and the high-precision measurement becomes more challenging [2].

2) In SiC MOSFETs, switch operational parameters, such as $R_{\rm DS-on}$, ON-state voltage drop ($V_{\rm DS-on}$), gate input capacitor ($C_{\rm rss}$), total gate charge (Q_g), diode reverse recovery time $t_{\rm GP}$, etc., are considerably smaller in value in comparison to those of Si-based MOSFETs and IGBTs. Detection of degradation based on the small value signals may lead to erroneous results.

3) The employed failure precursor should provide real-time degradation prognosis capabilities in order to be used in sensitive applications. To achieve this, the developed CM system should demonstrate noise-robustness and high-voltage capabilities to be used without the physical removal of the switch from the power electronic system [11]. $V_{\rm th}$ and drain leakage current as the failure precursors, for example, are commonly evaluated while the switch is interrupted from normal operation [4]. Some methods have the potential of online operation; however, the complication in implementation is a challenge of using them in real applications [12]. When the switch is float, for example, the indicators are increasingly difficult to be measured and employed for CM purposes.

4) For long-term health monitoring assessment, the employed measurement system should be highly robust against degradation. Due to high-frequency and high-voltage circuit design in SiC MOSFET-based circuits, the problem of measurement system aging is even more crucial. For some long-duty applications, the embedded components in the CM system are expected to assess the reliability level of the switch for a long period (several years) [5].

One of the main advantages of SiC MOSFET is faster turn-ON and turn-OFF dynamics. The switch transient behavior is considerably affected during the gate oxide degradation [11], [18]. In both planar [11] and trench-gate [11], [20] structures, the switch turn-ON and -OFF transient behavior is changed. Changes in $V_{\rm GP}$ and $t_{\rm GP}$ are extensively used as failure precursors in gate oxide degradation characterization. For example, in [6] and [11], using relatively large-value external gate resistance with the value of 100 Ω, the overall change of $t_{\rm GP}$ during the transition from brand-new condition to degraded condition is characterized. In the circuits with smaller gate resistance values (which is the case in realistic switching circuit designs), $t_{\rm GP}$ value is smaller, and hence, detection of its change during degradation is difficult [6]. To use $t_{\rm GP}$ as a degradation precursor, a measurement technique with a minimum time resolution of a few nanoseconds is required. In [6], a microcontroller with 300-ps time resolution is employed to measure the turn-ON and turn-OFF times based on the drain–source voltage ($V_{\rm DS}$) waveform. To detect such a fast change in $t_{\rm GP}$, $V_{\rm GS}$ waveform must be employed along with a voltage-time resolution. The implementation of these is at best complicated and costly for high-voltage, high-frequency SiC designs.

In this article, a real-time CM technique is proposed for gate oxide degradation monitoring of SiC MOSFETs in high-frequency applications. The output signal of the proposed CM system ($V_{\rm CM}$) is a voltage signal with dc value and provides a high resolution of the gate oxide degradation level of the switch. The basic idea of the article is that due to very fast switch rise and fall times in SiC MOSFET-based circuits, there is a wide range of high-amplitude harmonics in the $V_{\rm DS}$ frequency spectrum. Any change in the rise or fall times of $V_{\rm DS}$ waveform leads to a major change in harmonic amplitudes of a specific frequency range in the $V_{\rm DS}$ frequency spectrum. Capturing and monitoring the voltage magnitude of that specific frequency envelope can provide a real-time insight of the gate oxide degradation level of the switch.

$V_{\rm CM}$ is measured using the diagnosis section of the proposed CM technique, which is a fully analog sampling circuit. $V_{\rm CM}$ is obtained based on a specific range of harmonic orders in the frequency spectrum of $V_{\rm DS}$. From the implementation point of view, a well-tuned *RLC* filter is designed and placed on a voltage sample of $V_{\rm DS}$ as a bandpass filter. To bypass the effect of degradation of the components in the diagnosis section, connections of the diagnosis circuit to the switch terminals are controlled based on the CM timing sequence ($t_{\rm CM}$), imposed by the CM control section. Using a degradation setup for gate oxide aging based on high electric field stress (HEFS) approach, a set of discrete SiC MOSFETs 650 V/22 A is degraded at various rates. The functionality of the proposed CM system is evaluated in different circuit operating points and different load types (resistive and inductive). In a 200 kHz, 217-V power circuit topology, $V_{\rm CM}$ shows a 68% change, meaning that the CM system can present a real-time high-resolution monitoring of the degradation process based on a dc voltage value. The main advantages of the proposed CM technique can be summarized as follows.

1) A high-resolution monitoring for gate oxide degradation in high-frequency (up to 200 kHz) SiC MOSFET switching circuits.
2) Using a dc voltage-based resolution for demonstrating the gate oxide degradation level to facilitate the measurement and implementation in high power rating applications.
3) Using periodic sampling technique, to prohibit the component degradation of the CM system.
4) Analog-based CM circuitry, which provides a highly reliable and cost-effective approach for long-term reliability assessment.
5) Real-time prognostic capabilities without any need to slow down the switch or physical removal of the switch from the power circuit.

The rest of the article is organized as follows. In Section II, gate oxide degradation process is studied, and the variations in the turn-ON and turn-OFF processes are investigated. In Section III, the $V_{\rm DS}$ frequency spectrum is analyzed and characterized during the degradation process. In Section IV, the proposed CM technique, including diagnosis and control sections, is described in details. In Section V, the performance of

the CM system during the gate oxide degradation is examined at various rates of degradation. Commercially available SiC discrete MOSFETs 650 V/22 A are used to examine the proposed CM approach for high-frequency operating conditions.

II. Gate Oxide Degradation Process

To achieve superiority in $V_{\rm th}$ and g_{fs} values, the gate oxide layer is designed to be thinner in SiC MOSFETs than their Si counterparts [21]. Oxide traps near the SiC–SiO_2 interface [also called Near-Interfacial Oxide Traps (NIOTs)] are three orders of magnitudes higher than the Si–SiO_2 interface [22]. NIOTs can potentially contribute to the charge trapping process. The channel electrons direct tunneling into the existing NIOTs is the origin of the gate oxide degradation in SiC MOSFETs [15], [23]. Since trapped electrons in NIOTs oppose the applied oxide electric field, a higher level of the electric field is formed across the oxide for channel inversion resulting in $V_{\rm th}$ increment.

A. Variation in $V_{\rm th}$ and Miller Plateau

The effect of the mentioned trapped charges on $V_{\rm th}$ of the switch is described in [23]

$$V_{\rm th} = V_{\rm th_0} + \frac{Q_{\rm NIOT}(t_{\rm stress})}{C_{\rm ox}} \tag{1}$$

where $V_{\rm th_0}$ is the initial value of the threshold voltage, $C_{\rm ox}$ is the specific gate oxide capacitance, and $Q_{\rm NIOT}(t_{\rm stress})$ is the total charge transferred into NIOTs after a stress time of $t_{\rm stress}$. Furthermore, $Q_{\rm NIOT}(t)$ can be written as [11]

$$Q_{\rm NIOT}(t_{\rm stress}) \cong \frac{eN}{2\beta}\left[ln\frac{t_{\rm stress}}{t_0} + \gamma\right] \tag{2}$$

where N is the arbitrary oxide trap density, e is the electron charge, t_0 is the initial tunneling transition time, β is the tunneling parameter related to the barrier height facing the tunneling electrons, and γ is Euler's constant.

From (1) and (2), it can be inferred that as the stress time increases, $V_{\rm th}$ changes, and this has a detectable effect on $V_{\rm GP}$ and the turn-ON and turn-OFF event timings. To find the overall change in the turn-ON and turn-OFF dynamics over the degradation process, the change in $V_{\rm GP}$ should be described as an effective parameter. The relation between $V_{\rm GP}$ and $V_{\rm th}$ is written as [24]

$$V_{\rm GP} = V_{\rm th} + \sqrt{\frac{I_D L_{\rm CH}}{\mu C_{\rm ox} Z}} \tag{3}$$

where I_D is the drain channel current, $L_{\rm CH}$ is the channel length, Z is the channel width, and μ is the channel carrier mobility. Since μ is a decreasing function with respect to $t_{\rm stress}$ [23], $V_{\rm GP}$ is an increasing function of $t_{\rm stress}$.

B. Variation in the Switch Turn-ON Miller Plateau Time ($t_{\rm GP-On}$)

In the turn-ON process, $V_{\rm DS}$ of the switch falls from the OFF-state blocking voltage ($V_{\rm Bus}$) to zero. During turn-ON, the gate–source capacitance ($C_{\rm GS}$) must be charged, and the gate–drain capacitance ($C_{\rm GD}$) must be discharged. The main part of $V_{\rm DS}$ decrement occurs when $V_{\rm GS}$ is constant, and the output current of the driver ($i_G(t)$) discharges $C_{\rm GD}$ (known as Miller plateau). $i_G(t)$ in the turn-ON process is described as

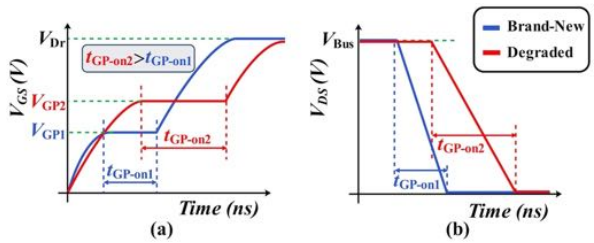

Fig. 1. (a) Increment in $V_{\rm GP}$ and $t_{\rm GP}$ and (b) decrement in $d(V_{\rm DS})/dt$ in turn-ON process during degradation.

$$i_G(t) = \frac{V_{\rm Dr} - V_{\rm GP}}{R_G} = -C_{\rm GD,avg}\frac{dV_{\rm DS}}{dt} \tag{4}$$

where $V_{\rm Dr}$ is the applied voltage from the gate driver to the gate–source of the switch, R_G is the sum of the internal and external resistances of the gate, and $C_{\rm GD,avg}$ is the average of the gate–drain capacitance of the switch. Assuming $V_{\rm DS}$ falls linearly from $V_{\rm Bus}$ to 0 V during switch turn-ON process, (4) is rewritten as

$$t_{\rm GP-on} = R_G C_{\rm GD,avg}\frac{V_{\rm Bus}}{V_{\rm Dr} - V_{\rm GP}}. \tag{5}$$

$t_{\rm GP-on}$ strictly depends on the Miller plateau considering (5). Since $V_{\rm GP}$ increases due to gate oxide degradation [according to (3) and Fig. 1(a)], it can be concluded that $t_{\rm GP-on}$ also increases over the degradation process. As a result, $d(V_{\rm DS})/dt$ in turn-ON process of the switch is decreased during the degradation, as shown in Fig. 1(b).

C. Variation in the Switch Turn-OFF Miller Plateau Time ($t_{\rm GP-Off}$)

In the turn-OFF process, $V_{\rm DS}$ of the switch increases from a zero value to $V_{\rm Bus}$. To turn OFF the switch, the driver provides a zero-level voltage for the gate to discharge $C_{\rm GS}$ and charge $C_{\rm GD}$. The same as the turn-ON process, the major part of the changes in $V_{\rm DS}$ occurs in the Miller plateau. In this time interval, $V_{\rm GS}$ is approximately constant, and the driver current charges $C_{\rm DG}$. Accordingly, $t_{\rm GP-off}$ is described as

$$t_{\rm GP-off} = R_G C_{\rm GD,avg}\frac{V_{\rm Bus}}{V_{\rm GP}}. \tag{6}$$

Regarding (3), $V_{\rm GP}$ increases over the gate oxide degradation [see Fig. 2(a)], and $t_{\rm GP-off}$ decreases in the degradation process as the result.

D. Variation in Switch Turn-ON and Turn-OFF Delays

During the delay intervals in both turn-ON and turn-OFF processes, the driver current solely changes $V_{\rm GS}$, and $V_{\rm DS}$ remains unchanged. In the turn-ON delay interval, the driver increases $V_{\rm GS}$ from zero to $V_{\rm th}$ [25]. Therefore, the turn-ON delay ($t_{\rm D-on}$) is described as

$$t_{\rm D-on} = -R_G C_{\rm GS} \ln\left(1 - \frac{V_{\rm th}}{V_G}\right). \tag{7}$$

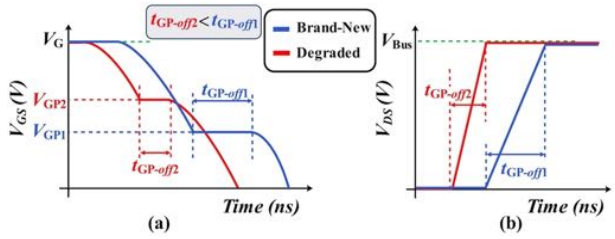

Fig. 2. (a) Increment in $V_{\rm GP}$ and decrement in $t_{\rm GP-off}$. (b) Increment in $d(V_{\rm DS})/dt$ in turn-OFF process during degradation.

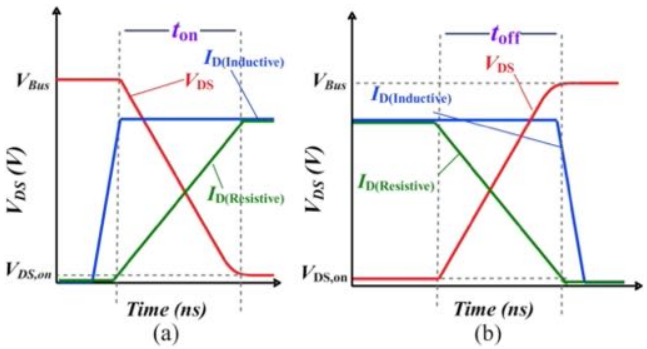

Fig. 3. $V_{\rm DS}$ and I_D waveforms of the switch in the resistive and inductive loads; (a) turn-ON and (b) turn-OFF transient behavior.

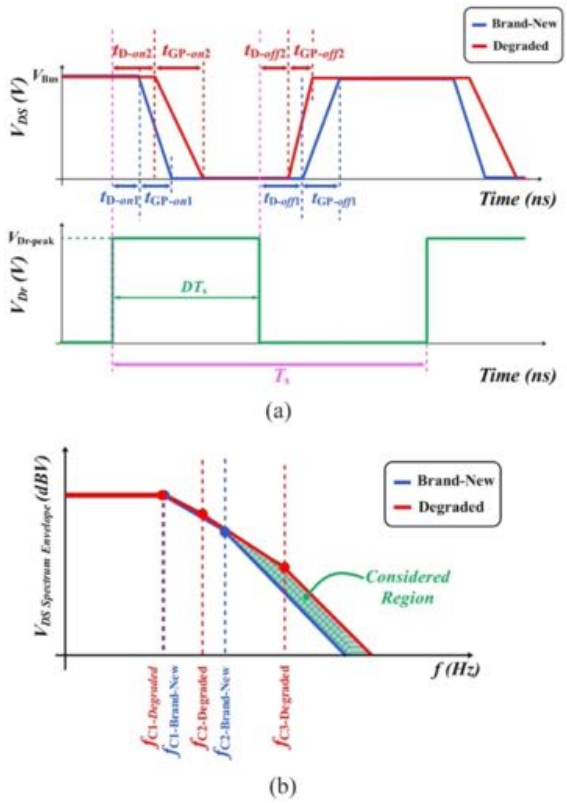

Fig. 4. (a) $V_{\rm DS}$ and (b) $V_{\rm DS}$ frequency spectrum of the degraded and brand-new condition of the switch.

In the turn-OFF delay interval, the driver current decreases $V_{\rm GS}$ from V_G to $V_{\rm GP}$ [25]. Thus, the turn-OFF delay ($t_{\rm D-off}$) is described as

$$t_{\rm D-off} = -R_G C_{\rm GS} \ln\left(\frac{V_{\rm GP}}{V_G}\right). \tag{8}$$

In the gate oxide degradation process, both $V_{\rm GP}$ and $V_{\rm th}$ values experience an increment. These changes have two effects: 1) based on (7), $t_{\rm D-on}$ is increased; and 2) based on (8), $t_{\rm D-off}$ is decreased. As a result, in the rising edge of $V_{\rm DS}$, related to the turn-OFF process of the switch, with a specific pulse width supplied by the gate driver, $V_{\rm DS}$ rise time will become shorter during the degradation.

Note that (5), (6), (7), and (8) are correct for the inductive load without any approximation. $V_{\rm GP}$ in turn-ON and turn-OFF transient time intervals is fixed. Because of the existence of the free-wheeling diode parallel to the inductive load, I_D is maintained constant when $V_{\rm DS}$ varies. This leads to having a constant value of $V_{\rm GP}$ over the turn-ON and turn-OFF transient time intervals. In resistive load, however, as I_D changes gradually with the change of $V_{\rm DS}$, $V_{\rm GP}$ is not a constant value based on (3). Therefore, some degree of approximation is needed to be considered if we want to use (5), (6), (7), and (8) equations for power circuits with resistive load. In Fig. 3, turn-ON [see Fig. 3(a)] and turn-OFF [see Fig. 3(b)] time intervals are shown for both resistive and inductive loads.

III. Spectrum Analysis of $V_{\rm DS}$ During Degradation

According to (5) and (7), there is a positive shift in $t_{\rm GP-on}$ and $t_{\rm D-on}$ in the degradation process. In addition, $t_{\rm GP-off}$ and $t_{\rm D-off}$ are decreased during the degradation. Fig. 4(a) depicts two typical $V_{\rm DS}$ waveforms in the brand-new and degraded conditions. The switching time period and duty cycle are shown as T_s and D, respectively. The frequency spectra of the waveforms in Fig. 4(a) are completely different, especially in high-frequency harmonics.

According to the work in [26], the frequency envelope of a symmetric trapezoidal waveform ($t_{\rm GP-on1} \approx t_{\rm GP-off1}$), namely $F(f)$, which is similar to $V_{\rm DS}$ waveform of the brand-new switch, can be written as

$$\text{Env}(F(f)) = 2DV_{\rm Bus}\text{sinc}(\pi f D T_s)\text{sinc}(\pi f t_{\rm GP-on}). \tag{9}$$

Applying $\log_{20}()$ function to both sides of (9), the spectral bounds can be established as

$$\begin{aligned} 20\log_{10}(\text{Env}(F(f))) &= 20\log_{10}(2DV_{\rm Bus}) - 180 \\ &+ 20\log_{10}\left|\text{sinc}(\pi f D T_s)\right| + 20\log_{10}\left|\text{sinc}(\pi f t_{\rm GP-on})\right|. \end{aligned} \tag{10}$$

The first term, i.e., $20\log_{10}(2DV_{\rm Bus})$, has a slope of 0 dB/dec and a level of $2DV_{\rm Bus}$. For small arguments, $\sin x = x$. Therefore, (11) can be written for different x values

$$\left|\frac{\sin x}{x}\right| \le \begin{cases} 1, & \text{for small } x \\ \frac{1}{|x|}, & \text{otherwise.} \end{cases} \tag{11}$$

Based on simplification in (11), for second and third terms of (10), two linear asymptotes can be considered. The first one with a slope of 0 dB/dec, and the second one with a slope of -20 dB/dec are the two considered asymptotes. On this basis, the term $20\log_{10}|\text{sinc}(\pi f D T_s)|$ has an asymptote

with a slope of 0 dB/dec and an asymptote with a slope of -20 dB/dec. These asymptotes intersect at $f = 1/\pi DT_s$. The third term in (10), i.e., $20\log_{10}|\mathrm{sinc}(\pi f t_{\mathrm{GP-on}})|$, also has an asymptote with a slope of 0 dB/dec and an asymptote with a slope of -20 dB/dec. These two asymptotes intersect at $f = 1/\pi t_{\mathrm{GP-on}}$. The spectral bounds of the V_{DS} frequency spectrum, therefore, consist of a three-segment line with two breakpoints. The first segment has a slope of 0 dB/dec. The second segment, starting at $f = 1/\pi DT_s$, has a slope of -20 dB/dec. The third segment, starting at $f = 1/\pi t_{\mathrm{GP-on}}$, has a slope of -40 dB/dec. Therefore, the envelope of the frequency-domain functions in (9) is described by three linear asymptotes having gradients of 0 dB/dec, -20 dB/dec, and -40 dB/dec in order of increasing frequency. The corner frequencies in which the mentioned asymptotes intersect (f_{c1} and f_{c2}) depend on the signal pulsewidth (DT_s) and rise time ($t_{\mathrm{GP-on}}$) as defined in

$$f_{c1} = \frac{1}{\pi DT_s}$$
$$f_{c2} = \frac{1}{\pi t_{\mathrm{GP-on}}}. \tag{12}$$

In the degradation process, the degraded switch exhibits an asymmetric trapezoidal waveform with different rising and falling times ($t_{\mathrm{GP-on2}} > t_{\mathrm{GP-off2}}$). The spectrum envelope of this waveform, namely $G(f)$, can be expressed by [27]

$$\mathrm{Env}(G(f)) = \Big|2DV_{\mathrm{Bus}}\left[\mathrm{sinc}(\pi f D t_{\mathrm{GP-on}})e^{j\pi f DT_s} - \mathrm{sinc}(\pi f t_{\mathrm{GP-off}})e^{-j\pi f DT_s}\right]\Big|. \tag{13}$$

For the spectrum envelope of $G(f)$, a new corner frequency is needed to be defined as

$$f_{c3} = \frac{1}{\pi t_{\mathrm{GP-off}}}. \tag{14}$$

According to the findings in [27], the profile of the envelope in (13) can be described as follows: In the frequency band of $[0, f_{c1}]$, there is a constant trend in the magnitude of all harmonic orders. In the frequency band of $[f_{c1}, f_{c2}]$, the harmonics magnitudes are decreased with a -20 dB/dec slope. The slope in the frequency band of $[f_{c2}, f_{c3}]$ is also -20 dB/dec; however, there is a constant attenuation ($\sim$-6 dB/dec) in the mentioned band. For the frequencies more than f_{c3}, the harmonics amplitudes are decreased with a slope of -40 dB/dec. Therefore, the frequency spectrum envelopes of the brand-new and degraded conditions of the switch can be plotted as Fig. 4(b). Accordingly, a discrepancy in V_{DS} spectrum in brand-new and degraded conditions can be expected in the high-frequency region, as indicated in Fig. 4(b). As noticed, the considered region widens while the switch degrades, and the discrepancy in high-frequency contents of V_{DS} becomes considerable. Therefore, a CM precursor based on the difference in high-frequency content of the V_{DS} frequency spectrum can be found.

We have developed a PSPICE switch model to validate V_{DS} frequency spectrum differentiation in the brand-new and degraded conditions for resistive load ($R_L = 10\ \Omega$) and inductive load ($R_L = 3.4\ \Omega$ and $L_L = 220\ \mu$H). The power circuit specifications of this case study are summarized in Table I. The degraded switch is simulated by increasing V_{th} in the switch model. Fig. 5 represents V_{DS} waveform in brand-new and degraded conditions. As noticed, the simulation result confirms the theoretical analysis, cf. Section II. The switch turn-ON time is increased in the degradation process while the turn-OFF time is decreased. These changes can be seen for both resistive load [see Fig. 5(a) and (b)] and inductive load [see Fig. 5(c) and (d)]. Basically, as V_{th} and V_{GP} values are increased due to the gate oxide degradation, the above-explained behavioral change is experienced in both resistive and inductive load. Fig. 6 shows the obtained frequency spectra of V_{DS} for brand-new and degraded conditions for resistive load simulation. As seen, the high-frequency contents of the spectra are considerably different.

TABLE I
SPECIFICATIONS OF THE CASE STUDY CONCEDED FOR ANALYSIS OF V_{DS} FREQUENCY SPECTRUM

V_{Bus}	200 V
C_{Bus}	48 μF
T_s	5 μs
D	20%
V_{GP1}	8 V
V_{GP1}	12 V
Resistive load	R_L=10 Ω
Inductive load	R_L=3.4 Ω , L_L = 220 μH

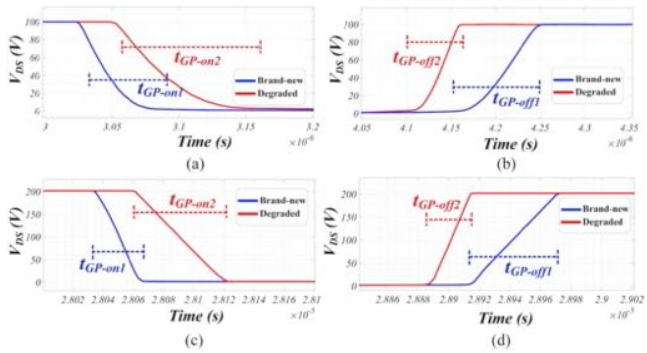

Fig. 5. PSPICE simulation results of the brand-new and degraded switch conditions; (a) turn-ON and (b) turn-OFF transient behavior with resistive load; (c) turn-ON and (d) turn-OFF transient behavior with inductive load.

IV. PROPOSED CM FOR GATE OXIDE DEGRADATION

A. Description

During the gate oxide degradation, the turn-ON and turn-OFF transients are altered due to the changes in V_{th} and V_{GP} values. Detecting these changes based on the V_{DS} voltage sample in power circuits with high-voltage switching operation needs a sensor voltage with very high-bandwidth capabilities, which leads to a complicated and costly technique. In the case study, cf. Section III, it was shown that for a waveform with very fast rise and fall time intervals (which is the usual case in SiC MOSFET-based circuits), a 35-ns change (50%) in the rise

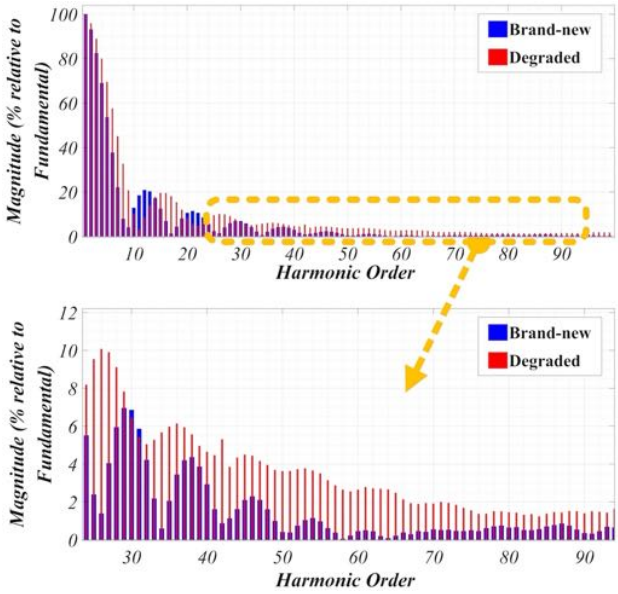

Fig. 6. $V_{\rm DS}$ frequency spectrum of the degraded and brand-new conditions in PSPICE simulation.

time value of the switch leads to major changes in the $V_{\rm DS}$ frequency spectrum, namely $V_S(f)$. In some harmonic orders, the amplitude is increased by the factor of 20. In Fig. 7, the $V_{\rm DS}$ frequency spectrum discrepancy is shown for brand-new and degraded conditions of the switch. Consider a case in which the frequency spectrum of $V_{\rm DS}$ experiences a significant change in amplitude of harmonic orders in the range of ith to jth ones. Monitoring V_S in this frequency range can be used as a gate oxide degradation indication. To achieve this, an analog bandpass filter ($H(f)$) is used to capture the above-mentioned frequency band. Rectification of the obtained signal can also lead to observing a magnified illustration of the changes in magnitude of this frequency envelope. On this basis, $V_{\rm CM}$ is defined as the average value of the rectified V_S signal in that specific frequency band, obtained as

$$V_{\rm CM} = \frac{1}{T_s}\int_0^{T_s}\left|\sum_{n=i}^{j} FT^{-1}\left[V_S(nf_s)\cdot H(nf_s)\right]\right| dt \qquad (15)$$

where f_s is the switching frequency, $H(f)$ is the transfer function of the employed filter, and $FT^{-1}()$ is the inverse Fourier transform. $V_{\rm CM}$ experiences a major change in switch transition from brand-new condition to the degraded condition. $V_{\rm CM}$, which is basically a dc voltage, can be presented as a precursor for high-resolution gate oxide degradation monitoring. In Fig. 7, a representation of step-by-step signal acquisition and analysis of the proposed CM technique is shown.

B. Operation Principle

In Fig. 8, the signal acquisition sequence in the proposed CM technique is shown. The detailed CM system overview, including *Diagnosis section* and *control section*, as the main two CM subsections, is shown in Fig. 9. The CM system is

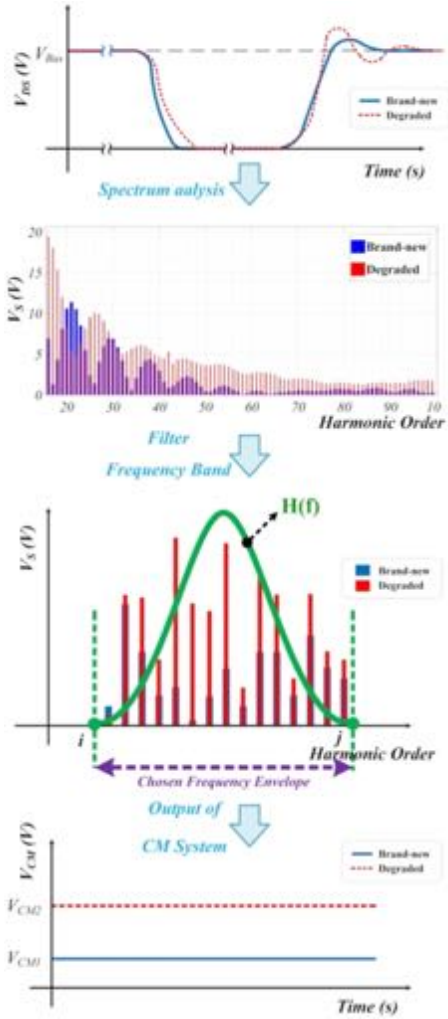

Fig. 7. Signal operation representation of the proposed CM process.

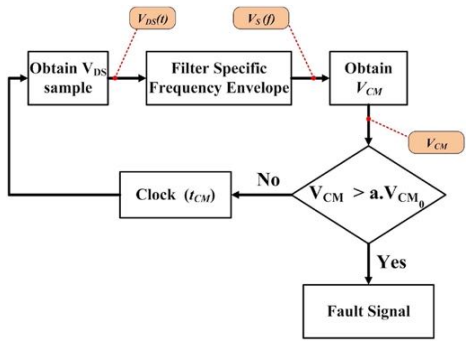

Fig. 8. Signal acquisition sequence in the proposed CM technique.

connected to high-voltage drain terminal in a limited time interval, based on the CM timing sequence ($t_{\rm CM}$) and imposed by the control section. Depending on the application, $t_{\rm CM}$ can be adjusted in the control section. When the control section sends the turn-ON command, the diagnosis section is activated for a specific time interval, and $V_{\rm CM}$ measurement is carried out. $V_{\rm CM_0} = V_{\rm CM}|t_{\rm stress=0}$ is defined as the reference value of $V_{\rm CM}$ in the brand-new condition of the switch. Safety factor,

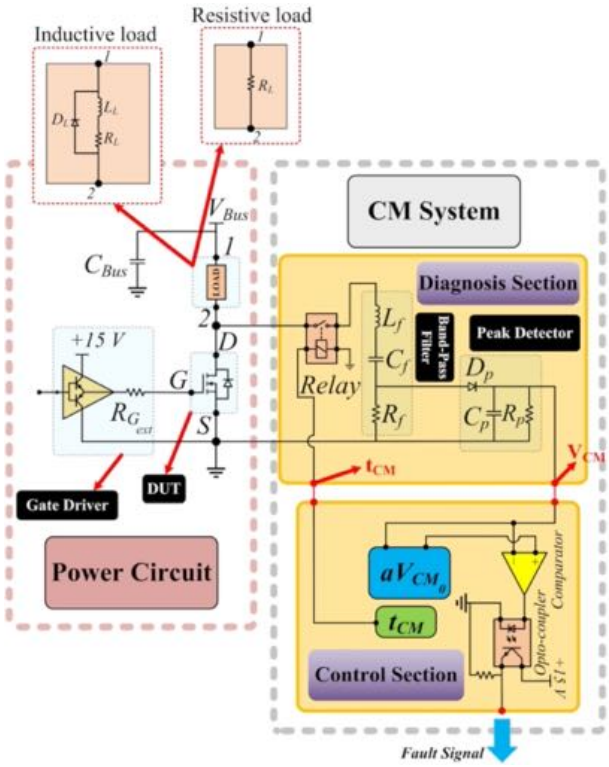

Fig. 9. Detailed view of the diagnosis and control sections of the proposed CM technique.

a, is defined, and $V_{\rm CM}{>}a.V_{\rm CM_0}$ enables the fault signal of the CM system. Because of gate oxide degradation effect on turn-ON and -OFF dynamics of the switch, $V_{\rm CM}$ has an increasing trend. Therefore, $a>1$, and the exact value of a depends on the sensitivity of the application. Using a, the degradation in early stages can be detected, and the catastrophic failure can be prohibited.

In Fig. 9, the circuit diagram of the proposed CM system is shown. The two main subsections of the CM system are described in the following.

1) Diagnosis Section: In this section, $V_{\rm DS}$ sampling and filtering are carried out. As explained, $V_{\rm CM}$ is obtained based on a specific range of harmonic orders in V_S signal. In this regard, a well-tuned *RLC* filter is designed and placed on a voltage sample of $V_{\rm DS}$ as a bandpass filter. Defining ith and jth harmonic orders of $V_S(f)$ as the lower (f_L) and higher (f_H) cutoff frequency values of the chosen frequency envelope, the inductance (L_f) and capacitance (C_f) values of the *RLC* filter are obtained based on

$$f_{\rm cr}=\frac{f_s(i+j)}{2}=\frac{1}{2\pi\sqrt{L_fC_f}} \tag{16}$$

where $f_{\rm cr}$ is the resonant frequency of the filter. A quality factor of the filter (Q_f) is a measure for indication of the filter's bandwidth (BW) relative to $f_{\rm cr}$, as shown in

$$Q_f=\frac{f_{\rm cr}}{\rm BW}. \tag{17}$$

For an *RLC* series tuned filter, (17) can be written as

$$Q_f=\frac{1}{R_f}\sqrt{\frac{L_f}{C_f}} \tag{18}$$

where R_f is the filter output resistance and has a deterministic role in the Q_f value of the filter. As Q_f is increased, the filter becomes more selective. Therefore, to have a proper selective filter in this design, $Q_f>10$ is considered. The filtered $V_{\rm DS}$ voltage sample is inserted into a peak detector to obtain $V_{\rm CM}$ based on (15). This leads to a higher value change on the output side, and a higher resolution of the gate oxide degradation level. Since the diagnosis circuit components are exposed to $V_{\rm Bus}$ during the sampling and measurement, degradation may be stimulated in these components, and change the components' operational parameters. Consequently, the CM system may provide erroneous results in long-term monitoring. To solve this problem, rather than leaving the CM detection circuit permanently connected and exposed to high-voltage stress and consequential aging, a relay is used to enable it as and when measurements are required.

2) Control Section: This subsection acts as the signal interface and decision-making system for the proposed CM technique. Any values higher than the defined threshold value will enable the fault alarm of the CM system. Moreover, an optocoupler is also used to achieve galvanic isolation for the exported fault command. The changing trend in $V_{\rm CM}$ can be mapped to the lifetime profile of the switch by using a proper failure model, which is the topic of another paper. This article is focused on using $V_{\rm CM}$ real-time value for monitoring the health status of the gate oxide layer during transitioning from brand-new condition to fully degraded condition.

As discussed in Section II, $t_{\rm D-on}$ and $t_{\rm D-off}$ values are also changed during the gate oxide degradation process. These changes majorly affect low-frequency content and dc value of $V_{\rm DS}$. The control unit of the converter usually regulates the dc value of $V_{\rm DS}$ for control purposes such as output voltage control. Therefore, changes in $t_{\rm D-on}$ and $t_{\rm D-off}$ are compensated by the closed-loop control of the converter. In adverse, the change in the transient times of the device depends on the gate drive system and usually is not affected by the control units. On this basis, the concentration of this article is on the high-frequency content of the $V_{\rm DS}$ frequency spectrum, which depends on the transient times of the device. The changes in pulsewidth of $V_{\rm DS}$, which can be compensated by the converter controller, has a negligible effect on $V_{\rm CM}$.

V. Experimental Verification

In this section, we use a dedicated degradation setup to degrade the SiC MOSFET case study switches in the gate oxide region, and investigate the performance of the proposed CM technique in various degradation rates and load current values.

In Table II, the circuit specifications and parameters are listed. $R_L=10\,\Omega$ is considered for the resistive load tests. $R_{G_{\rm ext}}$ is the external gate resistance (see Fig. 9). In Fig. 10, the laboratory setup of the direct switch structure and the CM system are shown. HIL is used for the CM control section and facilitates the verification of the CM system. It is worth emphasizing

TABLE II
OVERALL SPECIFICATIONS AND RATINGS OF THE IMPLEMENTED POWER CIRCUIT

V_{Bus}	93 V to 232V
C_{Bus}	34 μF
f_s	200 kHz
D	10%
$R_{G_{ext}}$	10 Ω
Resistive Load	R_L=10 Ω
Inductive Load	R_L=3.4 Ω , L_L = 220 μH

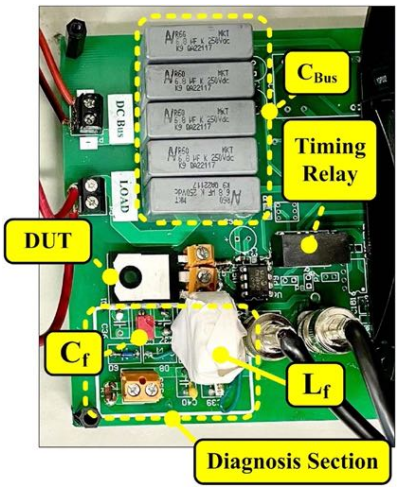

Fig. 10. PCB implementation of the direct switch circuit and the proposed CM system.

that the employed HIL is not an intrinsic part of the proposed CM technique, but it is used in this article for facilitating the verification process of the proposed CM idea. In fact, a dedicated microprocessor is not needed for the proposed CM technique. From a practical point of view, the main processor of the system, which is responsible for controlling the switch, can also operate as the control section of the proposed CM technique of this article.

A. Degradation Setup

In the literature, two stressors are introduced for the gate oxide degradation, i.e., HEFS and high temperature stress [10], [11]. In this article, we have used the HEFS method for inducing gate oxide degradation in the SiC MOSFET case study switches. In Fig. 11, the employed degradation circuit, based on HEFS mechanism, is shown. Using different values of gate stressor voltage ($V_{\rm stress}$), the functionality of the proposed CM technique is examined. The gate oxide breakdown voltage of the SiC MOSFET case study switch is found as 39 V. In [7], it is shown that for a Si MOSFET with a similar gate structure and similar ratings, the breakdown voltage is 65 V that clearly demonstrates the vulnerability of the SiC MOSFET gate oxide layer against HEFS. Theoretically, smaller conduction band offset between SiC and SiO_2 leads to higher leakage current and, hence, smaller breakdown field value [28].

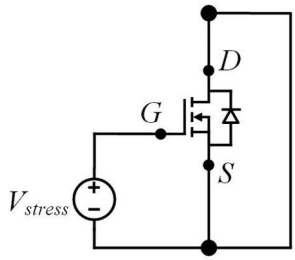

Fig. 11. HEFS circuit for gate oxide degradation.

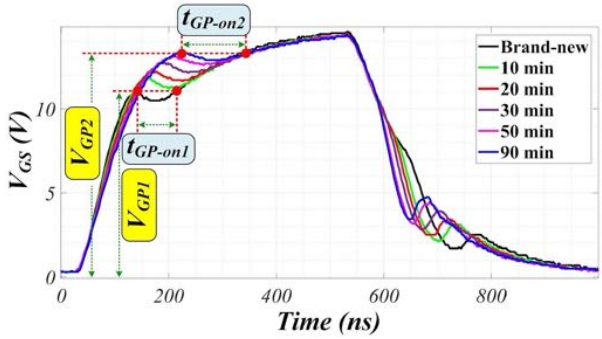

Fig. 12. $V_{\rm GP}$ and $t_{\rm GP-on}$ changes during the gate oxide degradation tests with $V_{\rm stress} = 37$ V.

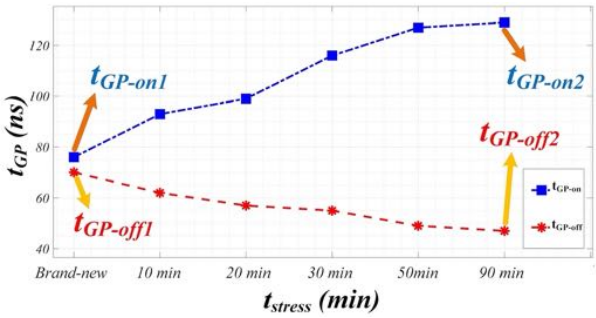

Fig. 13. $t_{\rm GP}$ changes in rising and falling edges of $V_{\rm GS}$ over gate oxide degradation in $V_{\rm stress} = 37$ V.

Based on the gate breakdown voltage of the switch, $V_{\rm stress}$ is chosen as 37 V, 37.5 V, and 38 V for the experimental evaluation of the proposed CM technique. To bypass the effect of temperature in the process of gate oxide degradation, all the degradation tests are carried out at room temperature level (26 °C) while switch case temperature is also 26 °C. In Fig. 12, the effect of degradation on $V_{\rm GP}$ and $t_{\rm GP-on}$ of the switch is shown in $V_{\rm stress} = 37$ V and stress time of 90 min. It can be seen that the $V_{\rm GP}$ value is changed from $V_{\rm GP1} = 11.9$ V to $V_{\rm GP2} = 13.4$ V due to gate oxide degradation. Moreover, in the turn-ON transient, $t_{\rm GP-on}$ has experienced a value change from 68 ns to 114 ns. The overall changes in $t_{\rm GP}$ value in the rising edge (i.e., $t_{\rm GP-on}$) and falling edge (i.e., $t_{\rm GP-off}$) of $V_{\rm GS}$ are shown in Fig. 13, which confirms the switch gate oxide degradation.

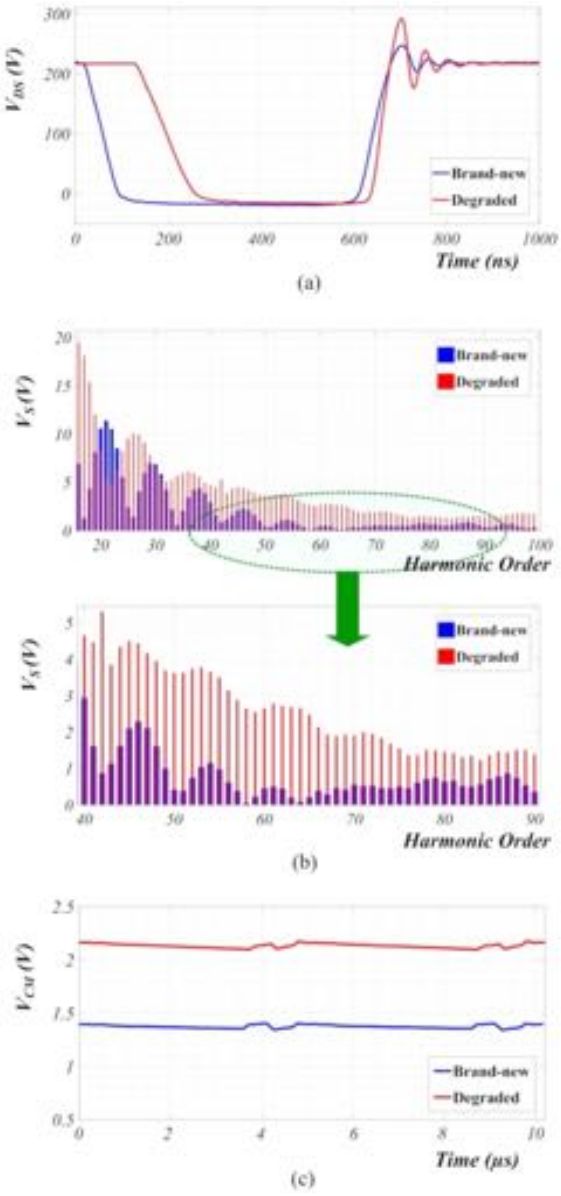

Fig. 14. (a) $V_{\rm DS}$ waveform in brand-new and degraded conditions with $V_{\rm stress} = 38$ V, (b) $V_{\rm DS}$ frequency spectrum changes due to HEFS, and (c) $V_{\rm CM}$ in HIL.

B. CM System Design

The case study switch is stressed in the gate oxide region with $V_{\rm stress} = 38$ V and a duration of 90 min. $V_{\rm DS}$ waveform and its frequency spectrum in new and degraded conditions are shown in Fig. 14(a) and (b), respectively. As noticed, the highest magnitude change is detected in the harmonic orders of $40{\rm th}$ to $90{\rm th}$. For example, in harmonic order of 58, the magnitude is increased by a factor of 54 from brand-new condition to degraded condition. Therefore, we choose this frequency envelope as the filtered chosen frequency band. Based on (16) and (18), C_f, L_f, and R_f are obtained as 33 pF, 4.7 μH, and 27Ω, respectively. In Fig. 15, the laboratory setup, including the direct switch PCB board, dc power supply, resistive load, inductive load, and HIL system, is shown.

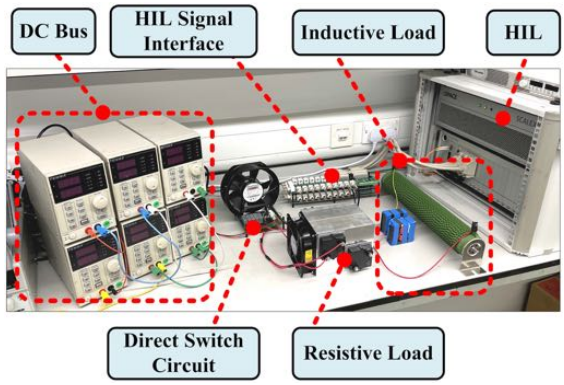

Fig. 15. Overall view of the implemented laboratory setup.

The sampling rate is adjusted as 10 ms in each 1 min. This is applied by $t_{\rm CM}$ signal, which is generated by HIL system running as the control section. $V_{\rm CM}$ is shown for the brand-new and degraded conditions in Fig. 14(c). $V_{\rm CM}$ value is changed from 1.35 V in brand-new condition to 2.1 V in degraded condition, meaning that a 55.5% value change is detected by the proposed CM system.

For higher-voltage operation of the switch, the evolution of the proposed CM technique is mostly related to the diagnosis section of the CM system. RLC filter components, i.e., C_f and L_f should be such designed to be able to handle the accumulated voltage amplitudes of the chosen frequency band of V_S. Peak detector subsection, including D_p, C_p, and R_p are not changed considerably in terms of voltage rating, as they are exposed to the filtered $V_{\rm DS}$ voltage.

C. Inductive Load Test

Testing the functionality of the proposed CM technique in inductive load is required to ensure that the proposed CM precursor for gate oxide degradation monitoring is functional in common converter typologies as well. In Fig. 15, the employed inductive load ($R_L = 3.4\ \Omega$, $L_L = 220\ \mu$H) is shown. R_L and L_L values are designed: a) based on the allowable load current of the experimental setup, and b) to mimic the process of the charging/discharging mechanism of the inductor in dc/dc converter topology.

The developed gate oxide degradation setup is employed to degrade the gate oxide layer with $V_{\rm stress} = 37.5$ V. The variations in turn-ON and turn-OFF transients of the switch due to the gate oxide degradation in $V_{\rm Bus} = 232$ V are shown in Fig. 16. At the beginning of the turn-ON transient time in inductive load tests, $V_{\rm DS}$ fall time shows a slowed-down behavior, which is due to the power path parasitic inductance out of the free-whiling diode path. This inductance acts similar to an ON-state snubber and does not allow I_D of the switch to have an instant incremental change. Accordingly, at the beginning of the turn-ON process, the current of the parasitic inductance starts increasing. Its voltage is proportional to the integration of its current and approximately has a second-order profile. Thus, $V_{\rm DS}$ will have two slopes at the beginning, if parasitic inductance values of the path are considerable.

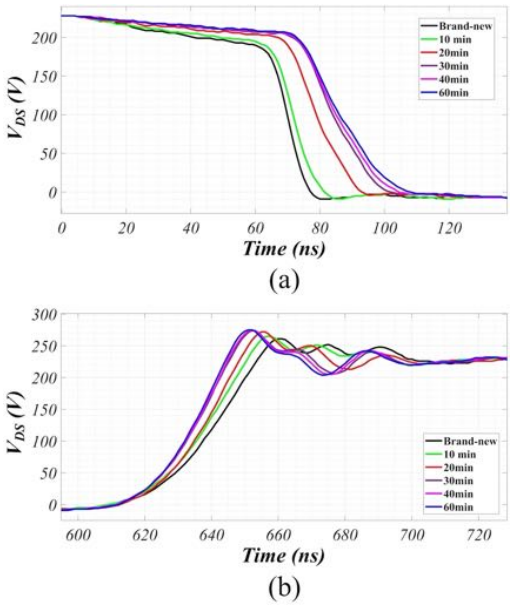

Fig. 16. $V_{\rm DS}$ changes during gate oxide degradation test with $V_{\rm stress} = 37.5$ V and $V_{\rm Bus} = 232$ V in inductive load; (a) turn-ON transient and (b) turn-OFF transient.

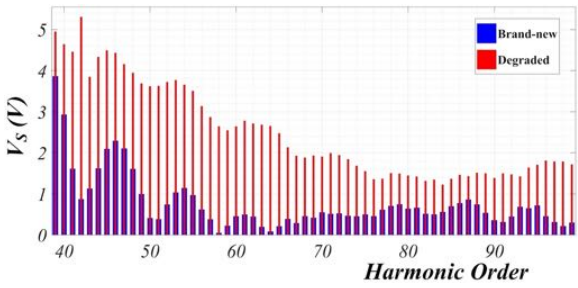

Fig. 17. Frequency spectrum of $V_{\rm DS}$ waveform in brand-new and degraded conditions in inductive load tests.

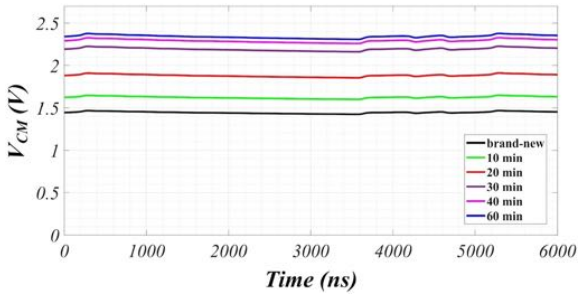

Fig. 18. $V_{\rm CM}$ changes over gate oxide degradation with $V_{\rm stress} = 37.5$ V and $V_{\rm Bus} = 232$ V in inductive load tests.

During the full course of degradation, the rise time value of the switch has changed from 73 ns to 108 ns, and fall time has changed from 54 ns to 45 ns. The $V_{\rm DS}$ frequency spectrum variations due to gate oxide degradation are shown in Fig. 17.

As can be seen in Fig. 17, all the high-frequency envelope of the $V_{\rm DS}$ frequency spectrum has experienced an amplitude increment. We choose harmonic orders of 42 to 96 as the chosen frequency envelope of the CM technique. Based on (16), (17), and (18), C_f, L_f, and R_f are obtained as 40 pF, 4.7 μH, and 27 Ω respectively. In Fig. 18, $V_{\rm CM}$ is shown for the test with inductive load.

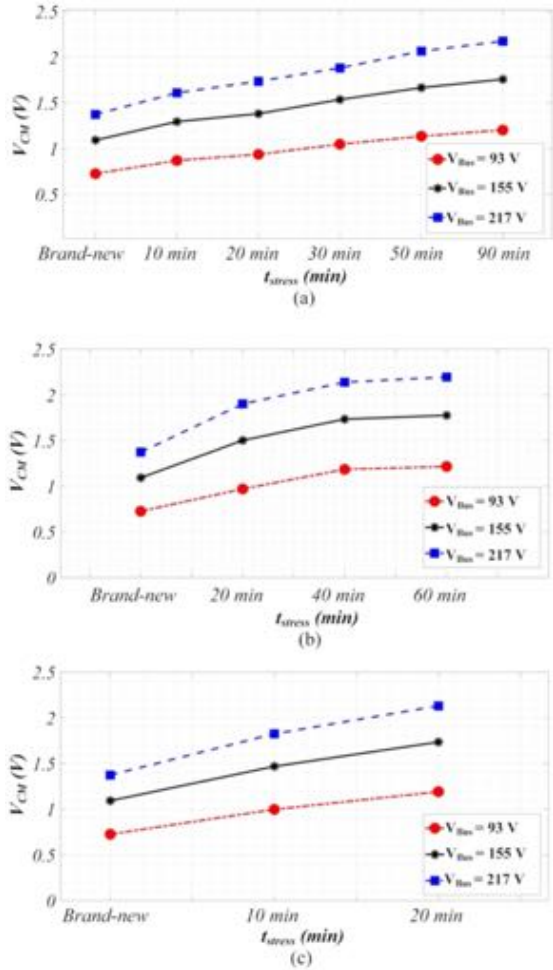

Fig. 19. $V_{\rm CM}$ value for (a) $V_{\rm stress} = 37$ V, (b) $V_{\rm stress} = 37.5$ V, and (c) $V_{\rm stress} = 38$ V for the three different $V_{\rm Bus}$ values.

D. Results and Discussion

All of the degraded switches are examined in a power circuit with three different $V_{\rm Bus}$ levels, i.e., 93 V, 155 V, and 217 V. As the employed resistive load is kept unchanged, the functionality of the proposed CM technique can be examined in three different load current levels as well. In Fig. 19, the effect of gate oxide degradation in $V_{\rm stress} = 37$ V, $V_{\rm stress} = 37.5$ V, and $V_{\rm stress} = 38$ V is shown in three different power circuit ratings. As seen, $V_{\rm CM}$ has a steady increasing trend during the stress time. Although a similar frequency envelope is filtered in all the $V_{\rm DS}$ levels, both the initial value and the magnitude changes in $V_{\rm CM}$ are different for different $V_{\rm DS}$ voltage levels. This is due to the different magnitudes in the frequency spectrum of the new and degraded switch. The $V_{\rm CM}$ change rate has a relatively linear profile [see Fig. 19(a)] in which the switch experiences a longer stress time. The linear increment leads to a high-resolution reliability monitoring during the gate oxide degradation.

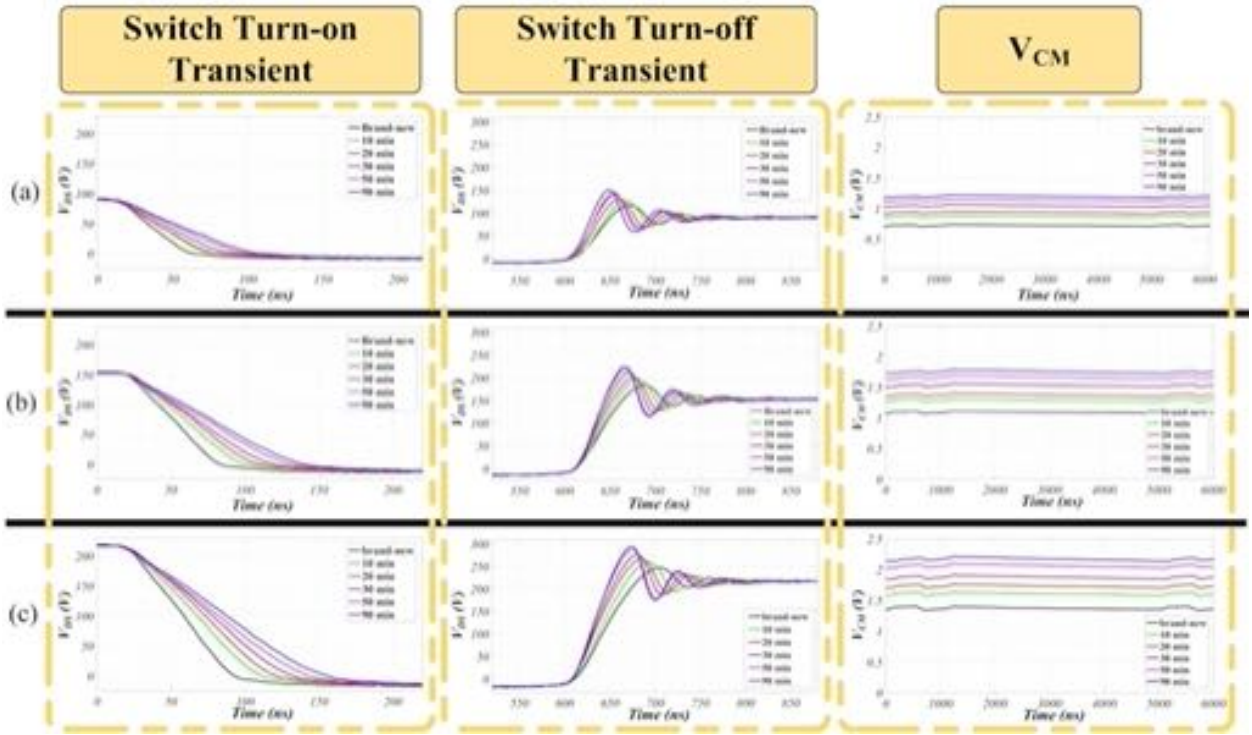

Fig. 20. $V_{\rm DS}$ and $V_{\rm CM}$ changes during the gate oxide degradation tests with $V_{\rm stress}$ =37 V and $V_{\rm Bus}$ = (a) 93 V, (b) 155 V, and (c) 217 V.

In Fig. 20, $V_{\rm DS}$ and $V_{\rm CM}$ waveforms are shown for the degradation tests with $V_{\rm stress} = 37$ V and three different $V_{\rm Bus}$ voltage levels. In all the tests, the rest of the circuit specifications, i.e., frequency, duty cycle, load impedance, etc., are identical and given in Table II.

Using the obtained data from the experimental tests, a failure factor, ψ, is defined as

$$\psi = \frac{V_{\rm CM} - V_{\rm CM_0}}{V_{\rm CM_0}} \times 100. \tag{19}$$

In all test conditions (see Fig. 21), ψ is monitored during the tests. When the switch performs in the brand-new condition, $\psi = 0$, indicating a healthy condition. During the gate oxide degradation, steady increment of ψ indicates the increasing probability of the gate oxide failure. The last data of each track are related to the ψ value in which the switch is failed in the gate oxide region. For example, for $V_{\rm stress} = 37$ V and $V_{\rm Bus} = 217$, $\psi = 59$, as shown in Fig. 21. This shows that the high rate of change in ψ is an accurate precursor for gate oxide failure. This is basically because of the high rate of change of $V_{\rm CM}$ during the gate oxide degradation process. Based on Fig. 21, it can be seen that the achieved resolution offered by the proposed method is about 60% to 68% while the achieved resolutions for $t_{\rm GP-on}$, $t_{\rm GP-off}$, $V_{\rm th}$, and $V_{\rm GP}$ are 60%, 40%, 20%, and 22%, respectively. Besides, without using costly and complicated measurement (e.g., microprocessor, etc.), based on fully analog diagnosis circuit, $V_{\rm CM}$ as a dc voltage resolution of gate oxide degradation can be used in noise-sensitive high-frequency SiC MOSFET CM.

E. Junction Temperature Effect on $V_{\rm CM}$

Examining the proposed CM technique in different temperature levels can verify its functionality in various operation modes of the switch. switch junction temperature (T_j) and switch case temperature (T_c) can be obtained as

$$P_{\rm loss} = \frac{T_j - T_c}{R_{jc}} \tag{20}$$

$$P_{\rm loss} = \frac{T_c - T_{Am}}{R_{\rm c-HS} + R_{\rm HS-Am}} \tag{21}$$

where $P_{\rm loss}$ is switch total power loss. $R_{\rm c-HS}$, $R_{\rm HS-Am}$, and R_{jc} are thermal resistance from case to heatsink, thermal resistance from heatsink to ambient, and thermal resistance from junction to case of the switch, respectively. Based on Table II and the operational parameters of the case study SiC MOSFET, $P_{\rm loss} = 7.41$ W.

To achieve two different values of switch junction temperature (T_j), two different heat dissipation topologies are implemented.

1) *Normal* T_j: A forced air-cooled heatsink with $R_{\rm HS-Am} = 0.07$ K/W is used. In this condition, $T_c = 34\,^{\circ}$C and $T_j = 45\,^{\circ}$C, as shown in Fig. 22(a).
2) *High* T_j: A small heatsink with relatively large value thermal resistance ($R_{\rm HS-Am} = 15.2$ K/W) with no air cooling is employed. In this condition, $T_c = 146\,^{\circ}$C and $T_j = 157\,^{\circ}$C, as shown in Fig. 22(b).

In Fig. 23, $V_{\rm CM}$ in brand-new and degraded conditions of the switch is obtained. For degrading the case study switch, we have used the developed gate oxide degradation setup in Section V-A of this article with $V_{\rm stress} = 37.5$ V. Both the brand-new and

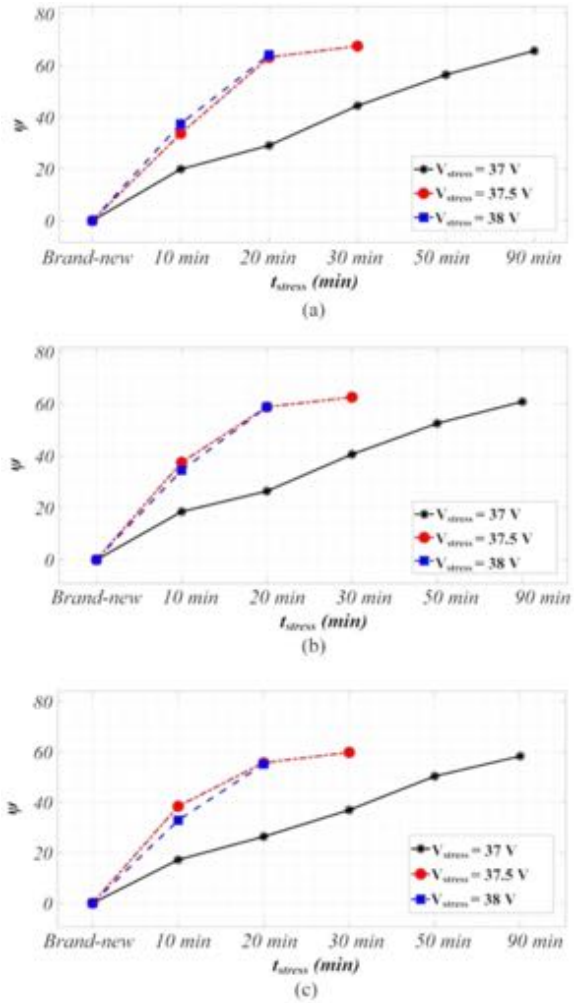

Fig. 21. ψ failure index in (a) $V_{\rm Bus} = 93$ V, (b) $V_{\rm Bus} = 155$ V, and (c) $V_{\rm Bus} = 217$ V tests.

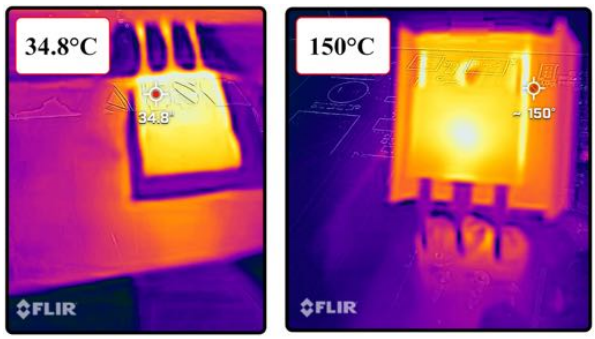

Fig. 22. Thermal images of the switch during operation in (a) $T_c = 34$ °C and (b) $T_c = 150$ °C.

degraded switches are employed in the two different heat dissipation topologies. It can be inferred that increment in T_j has not led to a major shift in $V_{\rm CM}$, as the shift is about 113 mV. Considering a 920 mV shift due to the gate oxide degradation in the case study tests of this article, the effect of temperature is not hindering $V_{\rm CM}$ to show the degradation level of the switch. Considering

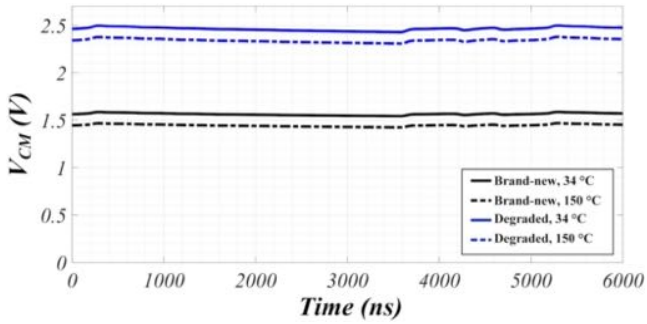

Fig. 23. $V_{\rm CM}$ changes due to temperature rise for brand-new and degrade conditions of the switch.

this, if the user is designing the proposed CM technique for an application, which is expected to have a large temperature rise (or fall), the minor shift in $V_{\rm CM}$ can be considered in the predefined safety factor, a, of the proposed CM technique to avoid erroneous fault signal.

VI. Conclusion

With a focus on SiC MOSFETs, a real-time high-frequency (up to 200 kHz) CM technique based on the $V_{\rm DS}$ frequency spectrum analysis of the switch was proposed in this article in order to provide high-resolution monitoring of the gate oxide degradation. It was shown that due to very fast-switching dynamics in SiC MOSFET operation, any change in the rise or fall times of the waveform leads to having a major change in a specific frequency envelope of this spectrum. Using the developed diagnosis circuit in the proposed CM system in this article, that specific frequency band envelope was used to produce a voltage signal with dc value, namely $V_{\rm CM}$, as a gate oxide degradation precursor. The proposed CM system was examined in different rates of gate oxide degradation and different power circuit ratings. The results showed that the dc value of $V_{\rm CM}$ signal experiences a 68% change in comparison to its initial value in the power circuit with $V_{\rm Bus} = 217$ V. Being fully analog and having a dc output signal, robustness against noise was achieved in high-frequency circuit conditions. In this regard, a high-resolution CM of gate oxide degradation can be developed using the proposed CM technique. Having fully analog-based design leads to having a highly reliable cost-effective CM system for long-duty applications.

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